An Overview on Twin-Flash™ Technology

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The usage of wireless applications like mobile smart phones, digital still cameras, video cam coders, PDA's is increasing dramatically. This drives the demand for high density and cost effective non volatile data storage media. Hard-disc micro drives and NAND-type flash's are the emerging dominant technologies for these applications. The flash products have the advantage of low power consumption and low weight but the disadvantage of higher cost per bit ratio for high density applications above 16MByte. The aggressive shrink path of the NAND technology allows shifting the boundary to higher densities. To increase the bit density multi-level NAND was introduced. Besides the NAND flash also with the Twin Flash a multi bit technology can be achieved. The technology benefits from the virtual ground NOR architecture and a more easy approach for two bits per cell separating physically the bits on each side of the Twin Flash device.

Infineon started the twin-flash technology in the 170 nm technology node with a 512Mb data-flash as lead product (1). The cell concept is a planar approach with a thick bit line-oxide as isolation for the bit-lines from the word-lines. The buried bit lines are shunted via borderless contacts and 1st metal lines to guarantee a homogeneous voltage supply for the cells during program & erase operation. The endurance and reliability characteristics of this array are excellent. Furthermore high cell efficiency could be achieved.
Shrinking the planar concept down to the 110nm node one drawback appears for the erase performance which can be adjusted by an array anti punch implant. In this case the cell width is limited by under diffusion and the break down voltage is reduced. In addition short channel effects can not be controlled by pocket implants like in normal n-MOS integration schemes.
To overcome this limitations a shallow trench isolated (STI) cell concept (2) is introduced. An anti-punch implant is no longer needed and short channel effects can be controlled like in standard n-MOS processes. The concept is first used for the 110 nm process node for a 1Gbit data flash device and can be shrunk further (3) down to the 60 nm node.
The integration of the STI cell requires the formation of local interconnects, which connect two active areas to the bit line. The self-aligned local interconnects have to be placed in minimum spaces between the word lines: reliable function of the local interconnects was demonstrated down to 80nm space between word lines, while the variation of contact resistance was kept small.
The optimization of the transistor based on state of the art n-MOS like construction yielded working devices down to 90nm gate length: Programming improved with smaller gate length. Key parameters for the cell operation such as 2nd bit effect, endurance and retention after cycling depend on the right choices for source/drain doping and spacer width, well and pocket implant and STI process parameters. We demonstrated feasibility of cell sizes down to 0,012um^2.
Improved endurance with smaller gate length and good retention was shown: a large window of more than 800mV between erased and programmed state after cycling and bake was achieved for cells of the 90nm node.
This work will review the shrink path of the STI cell down to 50nm generation and compare this cell to other options of planar cells, employing state of the art n-MOS like transistor construction. Also the extension of the cell down to the 40nm range will be discussed, including new options for 3 dimensional transistors.

(1) E. Maayan et. al.: ISSCC, (2002)
(2) J. Willer et. al.: VLSI Technology, pp. 76 (2004)
(3) N. Nagel et. al: VLSI Technology (2005)